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09/615,132	07/13/2000	Iain Robertson	TI-26019	6993

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Robert D Marshall Jr  
Texas Instruments Incorporated  
P O Box 655474 MS 3999  
Dallas, TX 75265

EXAMINER

SORRELL, ERON J

ART UNIT PAPER NUMBER

2182

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

12

**Office Action Summary**

Application No.

09/615,132

Applicant(s)

ROBERTSON, IAIN

Examiner

Eron J Sorrell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☒ Claim(s) 11 and 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 July 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-25 have been examined.

***Specification***

2. Please update the status of the pending U.K. Patent Application with an identification number.

***Claim Objections***

3. Claim 11 is objected to because of the following informalities: it appears as if the claim dependency is incorrect. It is the position of the Examiner that claim 11 should depend on claim 10 and not claim 1. Appropriate correction is required.
4. Claim 12 is objected to because of the following informalities: the preamble of the claim reads "the data transfer request of claim 11", however claim 11 is directed toward a data transfer controller. It is the position of the Examiner that this is a typographical error. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 10-12 and 25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 10 recites the limitation "said plurality of hubs" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is the position of the Examiner that this is a typographical error and the claim should read "said plurality of ports".

8. Referring to claim 25, it appears to the Examiner that the claim is contradictory to the parent claim 13. In claim 13 lines 25-34 seems to suggest that querying destination ports is required before a data transfer, however in lines 8-12 of claim 25 it is stated that the query is not performed. Appropriate clarification or correction is required.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1-18,24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (U.S. Patent No. 6,493,347) in view of Carn et al. (U.S. Patent No. 5,138,611).

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11. Referring to method claim 1, apparatus claim 7, and system claim 13, Sindhu et al. teaches a data transfer controller comprising:

a request queue controller receiving, prioritizing, and dispatching data transfer requests, each data transfer request specifying a data source, a data destination and a data quantity to be transferred (see item labeled 517 in figure 5A and lines 9-17 of column 6);

a data transfer hub connected to the request queue controller effecting dispatched data transfer requests (see item labeled 505 of figure 5A);

a plurality of ports, each of the plurality of ports having an interior interface connected to the data transfer hub and an exterior interface configured for external memory/device expected to be connected to the port, the interior interface operatively connected for data transfer therebetween (see lines 65-67 of column 2 and lines 1-9 of column 3); and

the data transfer hub controlling data transfer from a source port corresponding to the data source to a destination port corresponding to the data destination in a quantity to be transferred of a currently executing data transfer request (see lines 30-55 of column 3).

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Sindhu et al. fails to disclose the limitation that the data transfer hub further controls the source port and destination port to:

in response to a data transfer request, query the destination port to determine if the destination port is capable of receiving data of a predetermined size;

if the destination port is not capable of receiving data, waiting until the destination port is capable of receiving data;

if the destination port is capable of receiving data, reading data of a predetermined size from the source port and transferring the read data to the destination port.

Carn et al. teaches the limitations that Sindhu et al. fail to disclose (see lines 21-35 of column 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the controller of Sindhu et al. with the controller of Carn et al. such that the data transfer hub further controls the port and destination port to:

in response to a data transfer request, query the destination port to determine if the destination port is capable of receiving data of a predetermined size;

if the destination port is not capable of receiving data, waiting until the destination port is capable of receiving data;

if the destination port is capable of receiving data, reading data of a predetermined size from the source port and transferring the read data to the destination port. This modification would decrease packet loss due to an output port being busy as suggested by Carn et al.

12. Referring to method claim 2, apparatus claim 8, and system claim 14, Sindhu et al. discloses that each port includes at least one write reservation station for storing data prior to transfer to the external memory/device (see lines 17-28 of column 11);

the data transfer hub further controlling the destination port to determine whether any write reservation station of the destination port has not been allocated for receipt of data, and

if at least one write reservation station is not allocated for receipt of data, determining if the destination port can receive data and allocating a write reservation station for receipt of data (see lines 36-67 of column 11 and lines 1-6 of column 12).

13. Referring to method claim 3, apparatus claim 9, and system claim 15, Sindhu et al. discloses disallocating the write reservation station upon transfer of data from the write



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reservation to the external memory/device (see lines 17-35 of column 11).

Both Sindhu et al. and Carn et al. are silent on the controller transferring data from a write reservation station to the corresponding external memory/device at a data transfer rate of the external memory device, however Sindhu et al. does disclose methods for providing optimum performance (see lines 15-63 of column 22).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to further modify the system of Sindhu et al. such that data is transferred at the rate of the external memory/device because this would be the fastest data can be transferred with causing packets to be dropped.

14. As far as the examiner can interpret the claim in light of the 112 second paragraph rejection, claim 10 is rejected under 35 U.S.C. 103(a).

15. Referring to method claim 4, apparatus claim 10, and system claim 16, Sindhu et al. discloses a data transfer controller wherein each of the plurality of ports further includes an

identifier register corresponding to each reservation station  
(see lines 27-33 of column 7); and

the data transfer hub further controlling the destination  
port to allocate a write reservation station by writing  
identifier data in the corresponding identifier register (see  
lines 5-35 of column 11); and

store the read data in the write reservation station having  
a corresponding identifier stored in the identifier register  
corresponding to the write reservation station (see lines 5-35  
of column 11).

16. Referring to method claim 5, apparatus claim 11, and method  
claim 17, Sindhu teaches a data transfer controller wherein the  
data transfer controller is further capable of servicing a  
second transfer request between the source port and a second  
destination port while waiting until the destination port is  
capable of receiving data (see figure 2B). In figure 2B, there  
is a plurality of input sections (150-0 thru 150-3) coupled to  
an input switch (100), which forwards the data packets to a  
distributed memory (104). Output switch (102) then retrieves  
the packets from the distributed memory and forwards it to the  
appropriate output section. While the transfer from memory to

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the output switch is occurring, the input switch is capable of servicing a second transfer request.

17. Referring to method claim 6, apparatus claim 12, and system claim 18, the data transfer controller of Sindhu et al. as modified with the controller of Carn et al. as applied to claim 7 above is capable of controlling a second destination port to in response to a data transfer request, query the second destination port to determine if the second destination port is capable of receiving data of a predetermined size;

if the second destination port is not capable of receiving data, waiting until the destination port is capable of receiving data;

if the second destination port is capable of receiving data, reading data of a predetermined size from the source port and transferring the read data to the destination port (see lines 21-35 of column 5 of Carn et al.)

18. Referring to claim 24, both Sindhu et al. and Carn et al. fail to explicitly set forth the limitation that the data processors, the request queue controller, the data transfer hub and the plurality of ports are disposed on a single integrated circuit. It would have been obvious to one of ordinary skill in

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the art at the time of the applicant's invention to dispose all of the elements on an integrated circuit. It is common practice to fabricate application specific hardware on a single integrated circuit to minimize the amount of external connections.

19. As far as the examiner can interpret the claim in light of the 112 second paragraph rejection, claim 25 is rejected under 35 U.S.C. 103(a).

20. Referring to claim 25, Sindhu et al. discloses a data memory having a data transfer bandwidth on the same order as a data transfer bandwidth of the data transfer hub (see lines 65-67 of column 3 and lines 1-2 of column 4); and

a second port connected to the transfer hub and data memory (see figure 2B).

The controller of Sindhu et al. does not query a destination port to see if it is capable of receiving data.

21. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. in view of Carn et al. as applied to claims 1-18 above, and further in view of Godiwala et al. (U.S. Patent No. 5,629,950).

22. Referring to claim 19, Sindhu et al. teaches a system memory connected to a predetermined one of the plurality of ports (see item labeled 104 in figure 2B).

Both Sindhu et al. and Carn et al. are silent on the data processors including an instruction cache for temporarily storing program instruction and the data processor generating a data transfer for program cache fill from the system memory upon a read access miss to the instruction cache.

Godiwala et al. discloses a data processor comprising an instruction cache for temporarily storing program instructions controlling the data processor, and the data processor generating a data transfer for program cache fill from the system memory upon a read access miss to the instruction cache (see lines 41-67 of column 13).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to further modify the controller of Sindhu et al. such that the data processor further comprises an instruction cache for temporarily storing program instruction and the data processor generating a data transfer for program cache fill from the system memory upon a read access miss to the instruction cache. It is well known in

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the art that the use of caches increases performance by decreasing memory access times.

23. Referring to claims 20-23, Sindhu et al. teaches a system memory connected to a predetermined one of the plurality of ports (see item labeled 104 in figure 2B).

Both Sindhu et al. and Carn et al. are silent on the data processors including a data cache for temporarily storing data employed by the data processor, and the data processor generating a data transfer for write data allocation from the system memory to the data cache upon a read access miss, for data writeback cache fill from the system memory upon a write access miss to the data cache, and for data writeback to the system memory upon eviction of dirty data from the data cache.

Godiwala et al. discloses a data processor comprising an data cache for temporarily storing program data controlling the data processor, and the data processor generating a data transfer for write data allocation from the system memory to the data cache upon a read access miss, for data writeback cache fill from the system memory upon a write access miss to the data cache, and for data writeback to the system memory upon eviction of dirty data from the data cache (see lines 45-67 of column 11 and lines 1-28 of column 12).

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It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to further modify the controller of Sindhu et al. such that the data processor further comprises and data cache for temporarily storing program data. It is well known in the art that the use of caches increases performance by decreasing memory access times.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

The following U.S. Patents are cited to further show the state of the art as it pertains to data transfer controllers:

U.S. Patent No. 5,894,481 to Book

U.S. Patent No. 6,098,109 to Kotzur et al.

U.S. Patent No. 6,032,205 to Ogimoto et al.

U.S. Patent No. 5,909,594 to Ross et al.

U.S. Patent No. 5,924,112 to Barber et al.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J Sorrell whose telephone number is 703 305-7800. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffery A Gaffin can be reached on 703 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are 703 746-7239 for regular communications and 703 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

EJS

December 12, 2002

  
JEFFREY GAFFIN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100